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10/631,080	07/31/2003	Robert William Dobbs	200208890-1	2033

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EXAMINER	
CARPIO, IVAN HERNAN	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,080	DOBBS ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/4/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/31/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 11/4/2005 have been fully considered but they are not persuasive. The applicant argues that the Kan (US Patent 6250727) reference does not read on independant claims 1, 20, 28 and 30 because the Kan reference does not teach a circuit board with mounting pins that are directly mounted on the circuit board, examiner respectfully disagrees. Kan discloses a motherboard tray and though Kan does not specifically show the motherboard as an element in the figures it is inherent to the motherboard tray. The examiner reads the motherboard and motherboard tray, together, as the circuit board as is written in the rejection of independent claims 1,20,28 and 30>

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9,11-14 and 17-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kan.

With respect to claim 1 Kan teaches an apparatus, comprising: a circuit board (Fig. 1, element 8 along with column 1, lines 32 –36. Note that the circuit board is the motherboard tray along with the motherboard) that comprises one or more mounting pins (Fig. 1, elements 52,64,58 and 56) that are directly mounted on the circuit board with a chassis (Fig. 1, element 4).

With respect to claim 2 and with all the limitations of claim 1, Kan teaches that the chassis comprises one or more holes (Fig.1, elements 28) that comprise a diameter that is large enough to allow angled insertions (note: zero degrees is an angle also) of the on or more mounting pins, wherein on or more of the mounting pins are inserted (Fig. 3, note that element 56 is inserted into hole 28) into the one or more holes of the chassis to mount the circuit board into the chassis.

With respect to claim 3 and with all the limitations of claim 2, Kan teaches that the circuit board contains a first peripheral portion (Fig.1, on circuit board 8 the right edge) and a second peripheral portion (Fig.1, on circuit board 8, the left edge), wherein the first peripheral portion comprises the one or more pins (Fig.1, element 56) that are inserted into the one or more holes (Fig. 1, element 28) of the chassis, wherein the chassis with the one or more holes supports the first peripheral portion of the circuit board (Fig.3); wherein the chassis comprises a ledge (Fig. 1, element 20), wherein upon an abutment of the second peripheral portion with the ledge, the ledge supports (Fig.3, ledge 20 can be seen to support element 52) the second peripheral portion of the circuit board, wherein the circuit board is installed in the chassis free of card guide path sliding engagement of the circuit board.

With respect to claim 4 and with all the limitations of claim 3, Kan teaches that the apparatus further comprises a retainer component (Fig. 3, element 68), wherein the retainer component serves to hold the second peripheral portion against the ledge.

With respect to claim 5 and with all the limitations of claim 3, Kan teaches that the apparatus further comprises a retainer component (Fig. 3, note the top cover to hole element 28), wherein the retainer component serves to hold the one or more mounting pins in the one or more holes (Fig.3, the top of element 28 keeps pin 56 in hole 28).

With respect to claim 6 and with all the limitations of claim 2, Kan teaches that the one or more mounting pins comprise, one or more tabs (Fig. 1, element 56) that are directly mounted on the printed circuit board and connect the circuit board with the chassis, wherein the one or more holes of the chassis comprise one or more slots (Fig.1, element 28) to receive (Fig. 3) the one or more tabs.

With respect to claim 7 and with all of the limitations of claim 1, Kan teaches that the circuit board comprises a printed circuit board (column 1, lines 32-36) and the one or more mounting pins (Fig. 1, elements 52,64,58 and 56) that are directly mounted on the printed circuit board and connect the circuit board with the chassis, wherein the printed circuit board comprises a first peripheral portion (Fig.1, on circuit board 8 the right edge) and a second peripheral portion (Fig.1, on circuit board 8, the left edge); wherein a first mounting pin (Fig.1, element 56) of the one or more mounting pins is directly attached to the first peripheral portion (Fig.1, element 28), wherein a second mounting pin (Fig.1, element 52) of the one or more mounting pins is directly attached

to the second peripheral portion (Fig. 1, element 20). Note Figure 3 shows the attached setup.

With respect to claim 8 and with all the limitations of claim 7, Kan teaches that the chassis comprises one or more ledges (Fig. 3, element 28), wherein the one or more ledges comprises one or more recesses, wherein the second mounting pin (Fig. 3, element 52) on the second peripheral portion of the printed circuit board rests on a recess (Fig. 3, element 20) of the one or more recesses on one of the one or more ledges.

With respect to claim 9 and with all of the limitations of claim 8, Kan teaches that the apparatus further comprises one or more retainer components (Fig. 3, elements 68), wherein the one or more retainer components hold the first and second mounting pin against the chassis in recess to connect the circuit board with the chassis.

With respect to claim 10 and with all the limitations of claim 9, Kan teaches that the chassis comprises a chassis base (Fig.1, element 4) and a chassis cover component (Fig.3, element 68), wherein the chassis cover component comprises one or more a recesses (Fig. 3, element 68 note the recess formed all the way around element 68, leading to the head of 68), wherein upon connection of the chassis base and the chassis cover component, one or more of the one or more recesses of the chassis base component align with one or more of the one or more recesses of the chassis cover component (Fig. 3 note the recess of elements 68 aligns with recess 20 and with recess 28, and this hold the mounting pins on the chassis) to hold the second mounting pin.

With respect to claim 11 and with all the limitations of claim 7, Kan teaches that the first and second mounting pins (Fig.1, elements 56 and 52 respectively) protrude outside the perimeter of the printed circuit board.

With respect to claim 12 and with all the limitations of claim 11, Kan teaches that the chassis comprises a hole (Fig. 1, element 28) and a ledge (Fig.1, element 20), wherein the first mounting pin (Fig. 1, element 56) on the first peripheral portion of the printed circuit board is inserted (Fig. 3) into the hole in the chassis, wherein the second mounting pin (Fig.1, element 52) on the second peripheral portion of the printed circuit board rests on the ledge (Fig. 3).

With respect to claim 13 and with all the limitations of claim 12, Kan teaches that the ledge (Fig. 1, element 20) comprises one or more recess to receive (Fig. 3) the second mounting pin on the second peripheral portion of the printed circuit board.

With respect to claim 14 and with all limitations of claim 12, Kan teaches that the support of the first and second mounting pins by the hole and the ledge completes a mount (Fig.3) of the printed circuit board in the chassis free of card guide path sliding engagement of the printed circuit board.

With respect to claim 17 and with all the limitations of claim 1, Kan teaches that one ore more mounting pins comprise one or more integral formations (Fig. 1, elements 52 and 56) of a peripheral portion of the circuit board.

With respect to claim 18 and with all the limitations of claim 1, Kan teaches that the chassis comprises one or more holes wherein the one or more mounting pins and the one or more holes comprise a keying system. NOTE Fig. 3, pins 52 and 56 have to

be placed in a particular orientation with respect to the chassis so as to interact with elements 20 and 28 respectively and for the purpose of correctly mounting the circuit board (8) to the chassis (4), thereby comprising a keying system.

With respect to claim 19 and with all the limitations of claim 18, Kan teaches that the one or more pins are designed to only fit within the one or more holes if the one or more holes comprise a position, size, and shape that match a position, size and shape of the one or more mounting pins. NOTE Fig. 3, the position, size and shape of holes 28 and 20 match that of pins 56 and 52 respectively.

With respect to claim 20 Kan teaches a chassis (Fig.1, element 4) that comprises one or more holes (Fig.1, elements 28 and 20) to receive one or more mounting pins (Fig.1, elements 56 and 52) directly mounted on a circuit board (Fig. 1, element 8 along with column 1, lines 32 –36. Note that the circuit board is the motherboard tray along with the motherboard), wherein the one or more holes of the chassis allow the chassis to support (Fig.3) the one or more mounting pins to connect the circuit board with the chassis.

With respect to claim 21 and with all the limitations of claim 20, Kan teaches that one or more of the holes of the chassis comprises a diameter (Fig.2, element 20 note that the diameter allows angled insertion of mounting pin 52) that is large enough to allow an angled insertion of the one or more mounting pins into the one or more holes of the chassis.

With respect to claim 22 and with all the limitations of 21, Kan teaches one or more retainer components (Fig. 3, elements 68), wherein the one or more retainer

components hold the one or more mounting pins in the one or more holes of the chassis.

With respect to claim 23 and with all the limitations of claim 20, Kan teaches that the chassis with one or more holes supports a first peripheral portion (Fig. 3, element 28 supports element 56) of the circuit board; wherein the chassis comprises a ledge to support a second peripheral portion (Fig. 3, element 28 supports element 56) of the circuit board.

With respect to claim 24 and with all the limitations of claim 23, Kan teaches that the one or more mounting pins comprise one or more first mounting pins (Fig.1, element 56), wherein the second peripheral portion of the circuit board comprises one or more second mounting pins (Fig.1, element 52), wherein the ledge comprises one or more recesses (Fig.1, element 20) to receive the one or more second mounting pins, wherein the one or more recesses support (Fig. 3, element 20 supports element 52) the second peripheral portion of the circuit board.

With respect to claim 25 and with all the limitations of claim 24, Kan teaches one or more retainer components (Fig. 3, elements 68), wherein the one or more retainer components hold the one or more second mounting pins in the one or more recesses in the ledge to connect the circuit board with the chassis.

With respect to claim 26 and with all the limitations of claim 20, Kan teaches that the one or more holes are designed to only accept the one or more mounting pins of the circuit board if the one or more mounting pins align with the one or more of the one or

more holes (Fig.2, note that holes 28 will only accept pins 56 if they are aligned correctly).

With respect to claim 27 and with all the limitations of claim 26, Kan teaches that the one or more holes are designed to only accept the one or more mounting pins if the one or more mounting pins comprise a position, size, and shape that match a position, size and shape of the one or more holes. NOTE Fig. 3, the position, size and shape of holes 28 and 20 match that of pins 56 and 52 respectively.

With respect to claim 28 Kan teaches an apparatus comprising, means for attaching (Fig. 3, element 68) one or more mounting pins directly to a circuit board, and means for receiving (Fig.1, elements 28 and 20) the one or more mounting pin of the circuit board in a chassis, wherein the means for receiving the one or more mounting pins support the one or more mounting pins to connect the circuit board with chassis.

With respect to claim 29 and with all the limitations of claim 28, Kan teaches that the one or more mounting pins are located on a first peripheral portion (Fig.1, on circuit board 8 the right edge, elements 56) of the circuit board, wherein the means for receiving (Fig. 1, element 28) the one or more mounting pins support the first peripheral portion of the circuit board in the chassis, the apparatus further comprising means for supporting (Fig.1, element 20) a second peripheral portion (Fig.1, on circuit board 8, the left edge) of the circuit board in the chassis.

With respect to claim 30 Kan teaches a method comprising the step of inserting one or more mounting pins (Fig. 3, note mounting pin 56 is inserted into hole element

28) directly mounted on a circuit board into one or more holes in a chassis to connect the circuit board with the chassis.

With respect to claim 31 and with all the limitations of claim 30, Kan teaches that the one or more pins comprise one or more first mounting pins (Fig. 1, element 56) directly mounted on a first peripheral portion (Fig.1, on circuit board 8, the right edge) of the circuit board, wherein the chassis with the one or more holes (Fig.1, element 28) supports the first peripheral portion of the circuit board, the method further comprises the steps of, positioning one or more second mounting pins directly mounted on a second peripheral portion (Fig.1, element 52) of the circuit board to rest in one or more recesses on a edge (Fig. 1, element 20) of the chassis for support of the second peripheral portion of the circuit board, and retaining (Note the second peripheral portion is retained on the ledge by element 68 on figure 3) the second peripheral portion of the circuit board on the ledge of the chassis to hold the circuit board in the chassis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 16 rejected under 35 U.S.C. 103(a) as being obvious over Kan in view of Jansen (US Patent 6667889).

With respect to claim 15 Kan teaches all the limitations of claim 1 including the chassis holes and mounting pins, but Kan does not teach that the one or more mounting pins retract upon contact with the chassis, wherein one or more of the one or more mounting pins extend upon alignment with one or more holes of the chassis to engage with the one or more holes. Jansen teaches a pin (Fig. 5, element 72) that retracts upon contact with a chassis and that extends when aligned with a chassis hole. It would have been obvious to use the retractable pin taught by Jansen with the circuit board taught by Kan because this would protect the pin from breaking during attachment by absorbing pressure if the circuit board were to be installed to with too much force.

With respect to claim 16 and with all the limitations of claim 15, Jansen teaches that the mounting pins (Fig. 5, element 72) comprise one or more spring loaded (Fig. 5, element 74) extensions components.

Conclusion

Applicant's amendment necessitated the explanation in the grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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